REMARKS

Claims 1-25 are pending in the application. Claims 1 and 8 are rejected under 35 U.S.C. §103(a). Claims 2-7 and 9-14 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 15-25 are allowed. Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw all outstanding rejections.

I. REJECTIONS UNDER 35 U.S.C. § 103(a):

The Examiner has rejected claims 1 and 8 under 35 U.S.C. §103(a) as being unpatentable over Holloway et al. (U.S. Patent No. 6,747,996) (hereinafter "Holloway"). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. The Examiner has not provided any objective evidence or appropriate motivation for modifying Holloway to include an HPNA chip.

A *prima facie* showing of obviousness requires the Examiner to establish, *inter alia*, that the prior art references teach or suggest, either alone or in combination, all of the limitations of the claimed invention, and the Examiner must provide a motivation or suggestion to combine or modify the prior art reference to make the claimed inventions. M.P.E.P. §2142. The showings must be clear and particular and supported by objective evidence. *In re Lee*, 277 F.3d 1338, 1343, 61 U.S.P.Q.2d 1430, 1433-34 (Fed. Cir. 2002); *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000); *In re Dembiczak*, 50 U.S.P.Q.2d. 1614, 1617 (Fed. Cir. 1999). Broad conclusory statements regarding the teaching of multiple references, standing alone, are not evidence. *Id.*

The Examiner admits that Holloway does not teach an HPNA chip, as recited in claims 1 and 8. Paper No. 5, page 3. The Examiner's motivation for modifying Holloway to include an HPNA chip is "for higher density and less chip count for the same function as the design trend in the industry since it has been held by In re Larson, 340 F.2d 732, 93, 129 USPQ 23 (CCPA 1961)." Paper No. 5, page 3. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

In order to establish a *prima facie* case of obviousness, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 1994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1 and 8. *Id.*

Further, the Examiner's motivation ("for higher density and less chip count for the same function as the design trend in the industry") is not a motivation for modifying Holloway, which teaches synchronizing synchronous terminals with synchronous endpoints, each synchronous terminal and each synchronous endpoint having an asynchronous communications network coupled between at least one synchronous terminal and at least one synchronous endpoint (column 2, line 67 – column 3, line 5), to include an HPNA chip. The Examiner has failed to explain any connection between having higher density and less chip count and modifying Holloway to have an HPNA chip. Further, the Examiner has failed to explain any connection between having higher density and less chip count and modifying Holloway to send a null frame from the host Ethernet MAC to the HPNA chip prior to a data frame, as recited in claims 1 and 8. Neither has the Examiner explained any

connection between having higher density and less chip count and modifying Holloway to recognize the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs, as recited in claims 1 and 8. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1 and 8. *Id.*

B. *In re Larson* does not support modifying Holloway to include an HPNA chip.

As stated above, the Examiner cited *In re Larson* for supporting the modification of Holloway to include an HPNA chip. Paper No. 5, page 3. The Examiner had cited the citation of "340 F2d 732, 93, 129 USPQ 23 (CCPA 1961)." Paper No. 5, page 3. However, the cite of "129 USPQ 23" was a citation to *Ex parte Egan, Kister, and Scott.* Applicants believe that the Examiner meant to cite the citation of "340 F.2d 965, 968, 144 U.S.P.Q. 347, 349 (C.C.P.A. 1965)." If Applicants are citing the wrong citation, Applicants respectfully request the Examiner to provide the correct case cite.

Assuming that the Examiner meant to cite to 340 F.2d 965, 968, 144 U.S.P.Q. 347, 349 (C.C.P.A. 1965), Applicants respectfully assert that *In re Larson* does not provide support for modifying Holloway to include an HPNA chip. The court in *In re Larson* construed the term "integral" in a claim to include the constituent parts of a brake disc and clamp. *In re Larson*, 144 U.S.P.Q. at 349. The court held that while the brake disc and clamp of reference comprise several parts, they are rigidly secured together as a single unit; constituent parts are so combined as to constitute a unitary whole, which is "integral" within meaning of claim. *Id.* The court continued by holding that the term "integral" is not limited to a fabrication of parts from a single piece of metal, but is inclusive of other means for maintaining parts fixed together as a single unit; moreover, use of a one piece construction instead of the reference structure is a matter of obvious engineering choice. *Id.*

Applicants are confused as to the connection between the court in *In re Larson* interpreting "integral" and the Examiner's motivation to modify Holloway to include an HPNA chip. Applicants respectfully request the Examiner to clarify the connection pursuant to 37 C.F.R. §1.104(c)(2).

C. Holloway does not teach or suggest the following claim limitations.

Applicants respectfully assert that Holloway does not teach or suggest "a host Ethernet media controller and an HPNA chip" as recited in claim 1 and similarly in claim 8. The Examiner cites element 52 of Holloway as teaching a host Ethernet media controller and element 46b of Holloway as teaching an HPNA chip. Paper No. 5, page 2. Applicants respectfully traverse the assertion that Holloway teaches the above-cited claim limitation. Instead, Holloway teaches a telephone handset connected to a terminal which consists in part of a voice codec which converts between analog signals and sampled data signals at a sample rate as well as consists of a HPNA network interface 46a which assembles the voice samples into a packet which is then transmitted on an HPNA network to a gateway. Column 2, lines 29-36. Holloway further teaches that the gateway receives a HPNA packet at the counterpart HPNA network I/F 46b and queues it for transmission by Wide Area Network (WAN) interface 52. Column 2, lines 36-39. There is no language in Holloway that describes a wide area network interface as being equivalent to a host Ethernet media access controller as asserted by the Examiner. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that WAN interface 52 teaches a host Ethernet media access controller. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that WAN interface 52 teaches a host Ethernet media access controller, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143. Therefore, the Examiner has not presented a *prima facie* case of obviousness

in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Holloway does not teach or suggest "wherein control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 3, lines 11-13 of Holloway as teaching the above-cited claim limitation. Paper No. 5, page 2. Applicants respectfully traverse and assert that Holloway instead teaches that a synchronization protocol is established between a synchronous terminal and a synchronous end point by providing a gateway between the asynchronous communications network and the synchronous end point. Column 3, lines 5-8. Holloway further teaches that the gateway communicates with the synchronous terminal over the asynchronous communications network in accordance with the synchronization protocol. Column 3, lines 8-11. Holloway further teaches that the synchronization protocol includes sending a message (referred to as the "SP packet") from the gateway to the synchronous terminal where the SP packet contains a timestamp identifying a clock associated with the synchronous end point. Column 3, lines 11-15. Hence, Holloway teaches sending a packet that contains a timestamp from the gateway to the synchronous terminal. The Examiner has not provided any evidence that the SP packet that contains a timestamp discloses a control frame or a data frame or a control fame and data frame pair. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the SP packet that contains a timestamp teaches a control frame or a data frame or a control fame and data frame pair. *Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the SP packet that contains a timestamp teaches a control frame or a data frame or a control fame and data frame pair, and that it would be so recognized by persons of ordinary skill. *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *See In re*

Lee, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Furthermore, in connection with the rejection of the claim limitation recited in the above paragraph, the Examiner cites to the voice packet disclosed in Figure 17 as teaching a data frame and to the SP packet disclosed in Figure 17 as teaching a control frame. Paper No. 5, page 2. The Examiner has not provided any evidence that the SP packet and voice packet are pairs as required by the language recited in the above-recited claim limitation. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Holloway does not teach or suggest "sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 8, lines 3-7 of Holloway as teaching the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse and assert that Holloway instead teaches that if three packetized voice stations are active, then the gateway would signal in the SP packet that station 1 should preload its Backoff Level (BL) with 1, that station 2 should preload with 0 and that station 3 should preload with 2. There is no language in the cited passage that teaches sending a null frame. Neither is there any language in the cited passage that teaches sending a null frame from a host Ethernet MAC to the HPNA chip. Neither is there any language in the cited passage that teaches sending a null frame from the host Ethernet MAC to the HPNA chip prior to a data frame. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Holloway does not teach or suggest "recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 8, lines 3-7 of Holloway as teaching the above-cited claim limitation. Paper No. 5, page 3. Applicants respectfully traverse. As stated above, Holloway instead teaches that if three packetized voice stations are active, then the gateway would signal in the SP packet that station 1 should preload its Backoff Level (BL) with 1, that station 2 should preload with 0 and that station 3 should preload with 2. There is no language in the cited passage that teaches sending a null frame. Neither is there any language in the cited passage that teaches recognizing the null frame on a HPNA chip. Neither is there any language in the cited passage that teaches recognizing the null frame on a HPNA chip as an indication that a next received frame will be the data frame. Neither is there any language in the cited passage that teaches maintaining synchronization between the control frame and the data frame pairs. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in Holloway, and thus the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8. M.P.E.P. §2143.

II. ALLOWABLE SUBJECT MATTER:

Applicants thank the Examiner for the allowance of claims 15-25. Applicants further thank the Examiner for the indication of allowability of claims 2-7 and 9-14.

III. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 1-25 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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